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| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/671,585 | KITAGAWA, NOBUTAKA | |
| | Examiner | Art Unit | |
| | Dharti H. Patel | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an Amendment filed on 01/30/2006*.

2. ☒ The allowed claim(s) is/are *1-31*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 09/29/03, 02/17/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

***Information Disclosure Statement***

The references cited in the Information Disclosure Statements filed on September 29, 2003 and February 17, 2004 are acknowledged.

***Allowable Subject Matter***

The following is an examiner's statement of reasons for indicating allowance of claims 1 and 16: Nikutta et al. teaches an electrostatic discharge protection circuit device comprising a first electrostatic discharge protection circuit [Fig. 1, ESD 3] connected between a first external terminal supplied with a first power supply voltage [Fig. 1, VCC-2] at time of ordinary operation and a first ground terminal [Fig. 1, VSS-2]; a second electrostatic discharge protection circuit [Fig. 1, ESD-1] connected between a second external terminal supplied with a second power supply voltage [Fig. 1, VCC-1] at the time of ordinary operation and a second ground terminal [Fig. 1, VSS-1], the second electrostatic discharge protection circuit having substantially the same configuration as that of the first electrostatic discharge protection circuit.

However, the prior art does not disclose a trigger signal line which connects in common an output node of surge detection circuits of the first and second electrostatic discharge protection circuits, and transfers a surge detection output of one of the first and second electrostatic discharge protection circuits to the other electrostatic discharge protection circuit as a trigger signal; and a common discharge line connected directly to the first ground terminal, connected to the second ground terminal via a parallel circuit composed of a forward-connected parasitic diode element and a reverse-connected parasitic diode element, and used commonly by the first and second of

electrostatic discharge protection circuits. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

Liu et al. teaches ESD protection circuits for integrated circuits' mixed-voltage interface. Liu et al. teaches a first and second NMOS transistors [Fig. 7, N1, N2] arranged in parallel, both separately coupled to a first and second low voltage sources [Fig. 7, Vss1, Vss2] and fed by two different power supplies [Fig. 7, Vcc1, Vcc2]. A trigger signal line [Fig. 7, 410] to one transistor N1 is isolated from the trigger signal line [Fig. 7, 420] connected to the other transistor N2. Liu et al. discloses two separate trigger signal lines from transistors of two ESD protection devices, but does not disclose a trigger signal line which connects in common an output node of surge detection circuits of the first and second electrostatic discharge protection circuits.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
02/16/2006

PHUONG T. VU
PRIMARY EXAMINER